

The Political Economy of Semiconductor Supply Chains and Great Power Competition

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ABSTRACT

Semiconductors have become the defining strategic commodity of the twenty-first century, occupying a position in contemporary geopolitics analogous to that once held by oil. This paper offers an analytical political economy examination of how semiconductor supply chains have become both an instrument and a battleground of great power competition, with particular attention to the United States, China, Taiwan, and the emerging role of India. Drawing on global production network (GPN) theory, techno-nationalism, and strategic trade theory, the paper argues that the semiconductor industry's extreme specialization and geographic concentration have transformed ordinary commercial interdependence into a source of structural power and vulnerability. The paper traces the evolution of export control regimes such as the United States' 2022 and subsequent restrictions on advanced chip technology, China's countervailing industrial policy under initiatives comparable to the "Big Fund," and Taiwan's "silicon shield" strategy centred on TSMC. It then undertakes a detailed case study of India's semiconductor ambitions, examining the India Semiconductor Mission, the Production Linked Incentive scheme, and recent investments by Tata Electronics, Micron Technology, and CG Power, situating India's strategy within the broader "friend-shoring" and diversification logic pursued by Western governments. The analysis concludes that semiconductor geopolitics is producing a fragmented, bloc-oriented global technology order in which economic efficiency is increasingly subordinated to strategic autonomy, with significant implications for developing economies seeking to enter high-technology manufacturing. The paper contributes to the political economy literature by integrating emerging-market perspectives, particularly from India, into a field that has hitherto been dominated by US-China-Taiwan-centric analysis.

Keywords: *semiconductor supply chains, political economy, great power competition, export controls, India Semiconductor Mission, techno-nationalism, global production networks, technological sovereignty*

1. Introduction

Few industrial sectors illustrate the entanglement of economics and geopolitics as starkly as semiconductor manufacturing. Semiconductors, the foundational components of nearly every digital device, are simultaneously a commercial product traded in a competitive global market and a strategic asset whose control confers military, economic, and technological power. The industry's defining feature is its extraordinary degree of specialization and geographic concentration: chip design is dominated by a handful of American firms and design-software providers; the most advanced lithography equipment is produced almost exclusively by a single Dutch company, ASML; and the fabrication of the most advanced logic chips is concentrated overwhelmingly in Taiwan, principally through the Taiwan Semiconductor Manufacturing

Company (TSMC). This concentration, which decades of efficiency-seeking corporate strategy produced, has become a source of acute strategic anxiety for governments that depend on continuous access to advanced chips for defense systems, artificial intelligence development, and civilian technology industries.

The political economy of semiconductors has therefore moved from the periphery of trade policy to the center of great power strategy. The United States has progressively tightened export controls on advanced semiconductor technology to China, citing national security concerns related to artificial intelligence and military modernization. China has responded with an ambitious, state-directed effort to achieve self-sufficiency in chip design and fabrication, backed by enormous public investment funds. Taiwan's centrality to the global supply chain has become both a source of geopolitical leverage, often termed a "silicon shield," and a profound vulnerability given the island's contested status and its proximity to mainland China. Meanwhile, a wider set of governments, including the European Union, Japan, South Korea, and India, have launched their own subsidy programs and industrial strategies aimed at reducing dependence on any single geographic node in the supply chain.

This paper situates these developments within a political economy framework that treats semiconductor supply chains not merely as commercial networks optimized for cost and efficiency, but as sites of structural power in which control over critical nodes—chip design intellectual property, lithography equipment, advanced fabrication capacity, and raw material inputs—translates into geopolitical leverage. The analysis draws on global production network theory, which examines how value is created, captured, and governed across dispersed production stages, and on the concept of techno-nationalism, which describes the resurgence of state efforts to align technological capability with national security objectives.

A distinguishing contribution of this paper is its sustained attention to India's emerging role in this landscape. Much of the existing scholarly and policy literature on semiconductor geopolitics concentrates on the triangular relationship between the United States, China, and Taiwan, with South Korea, Japan, and the European Union treated as secondary actors. India has historically been peripheral to this literature despite being the world's most populous country and a rapidly growing electronics consumption market. However, since 2021 India has launched a series of ambitious policy interventions, including the India Semiconductor Mission (ISM), the Production Linked Incentive (PLI) scheme for electronics manufacturing, and targeted fiscal incentives that have attracted investment commitments from firms such as Micron Technology, Tata Electronics, CG Power, and Kaynes Technology. These developments make India an increasingly important case for understanding how "friend-shoring" and supply chain diversification strategies are reshaping the political economy of semiconductors beyond the traditional East Asian core.

The paper proceeds as follows. Section 2 reviews the relevant literature on strategic trade, global production networks, and techno-nationalism as it applies to semiconductors. Section 3 develops the theoretical framework guiding the analysis. Section 4 outlines the qualitative, document-based methodology employed. Section 5 examines the structure of the global semiconductor value chain and its key chokepoints. Section 6 analyzes the trajectory of United States-China technological rivalry and the evolving export control regime. Section 7 considers Taiwan's structural position and the silicon shield thesis. Section 8 provides a detailed case study of India's semiconductor strategy. Section 9 offers a comparative analysis across major and emerging semiconductor actors. Section 10 discusses the broader political economy implications of these dynamics, and Section 11 offers policy recommendations before the paper concludes.

2. Literature Review

2.1 *Strategic Trade Theory and Industrial Policy*

The economic rationale for state intervention in high-technology industries has a long lineage in strategic trade theory. Krugman (1986) and Brander and Spencer (1985) demonstrated that under conditions of imperfect competition and increasing returns to scale, government subsidies to domestic firms in strategic sectors can shift oligopolistic rents from foreign to domestic firms, generating welfare gains that classical free trade models do not capture. Semiconductor manufacturing, characterized by extraordinarily high fixed costs, steep learning curves, and network externalities, has long been regarded as a paradigmatic case for strategic trade intervention. Historical scholarship on the East Asian developmental state, notably Amsden's (1989) analysis of South Korea and Wade's (1990) study of Taiwan, demonstrated that state-directed credit allocation, export discipline, and technology transfer requirements enabled late-industrializing economies to establish globally competitive electronics industries within a generation.

2.2 *Global Production Networks and Global Value Chains*

A parallel literature, associated with Gereffi, Humphrey, and Sturgeon (2005) and later Yeung and Coe's (2015) global production network (GPN) framework, examines how transnational corporations coordinate dispersed production activities across multiple countries while retaining control over high-value activities such as design and branding. Applied to semiconductors, this literature illuminates the industry's characteristic vertical disintegration: the separation of chip design ("fabless" firms such as Qualcomm, Nvidia, and Apple), foundry fabrication (TSMC, Samsung, GlobalFoundries), equipment supply (ASML, Applied Materials, Tokyo Electron), and assembly, testing, and packaging (a stage in which firms in Malaysia, the Philippines, and increasingly India play a significant role). Fuller (2016) extended this analysis specifically to the semiconductor industry, arguing that the fragmentation of production has created multiple potential chokepoints that states can exploit for strategic leverage, a dynamic that has become increasingly salient since the mid-2010s.

2.3 *Techno-Nationalism and the Securitization of Technology*

A more recent body of scholarship examines the resurgence of techno-nationalism, defined broadly as the belief that technological capability is inseparable from national security and that states must therefore actively shape technological development rather than leaving it to market forces alone. Weiss (2014) traced the persistence of the "developmental network state" in advanced economies, showing that even liberal market economies such as the United States have long relied on defense-related public investment to sustain technological leadership. More recent work, including that of Farrell and Newman (2019) on "weaponized interdependence," argues that states occupying central positions within global networks—whether financial, informational, or technological—can convert that structural position into coercive leverage over rivals, a dynamic clearly visible in the United States' use of its control over chip design software and manufacturing equipment to restrict Chinese access to advanced semiconductors.

Miller's (2022) widely cited historical account traces the semiconductor industry's development from its Cold War origins to its current status as an object of great power rivalry, documenting how the industry's concentration in East Asia emerged from decades of cost-driven corporate decisions that inadvertently created acute strategic vulnerabilities for the United States and its allies. Complementing this account, Fuller and Ernst (2023) and other contributors to the emerging semiconductor political economy literature have examined China's response, particularly the role of state-guided investment funds and the limits of import substitution in advanced lithography and electronic design automation software.

2.4 India in the Global Electronics and Semiconductor Literature

India's position within this literature has historically been marginal, reflecting the country's limited role in global semiconductor manufacturing until the early 2020s. Existing scholarship on India's electronics sector, such as the work of Kathuria and colleagues at the Indian Council for Research on International Economic Relations (ICRIER), has focused primarily on mobile phone assembly under the PLI scheme and India's position within regional electronics value chains centered on China and Vietnam (Kathuria et al., 2021). Studies published by NITI Aayog (2021) and the Ministry of Electronics and Information Technology have documented the policy rationale for India's semiconductor push, emphasizing both import substitution and the strategic objective of reducing dependence on any single foreign supplier following the disruptions of the COVID-19 pandemic. However, systematic academic analysis integrating India's emergence into the broader comparative political economy of semiconductor competition remains limited, a gap this paper seeks to address.

2.5 Synthesis and Research Gap

The literature reviewed above establishes three complementary insights: first, those semiconductors possess economic characteristics that justify treating them as a strategic sector subject to legitimate state intervention; second, that the industry's global production network structure creates multiple points at which states can exercise coercive leverage; and third, that the securitization of technology has intensified state involvement in ways that increasingly override purely commercial logic. What remains underdeveloped is a systematic account of how these dynamics are reshaping opportunities and constraints for emerging economies such as India, which are simultaneously courted by established powers seeking diversification and constrained by their own limited technological base. This paper addresses that gap.

3. Theoretical Framework

This paper adopts an eclectic theoretical framework combining three complementary strands: global production network (GPN) theory, the concept of weaponized interdependence, and techno-nationalist industrial policy theory.

3.1 Global Production Networks and Structural Power

GPN theory conceptualizes production as organized through networks of firms, states, and institutions distributed across multiple national jurisdictions, coordinated by lead firms that capture disproportionate value through control over intangible assets such as design, intellectual property, and brand. Applied to semiconductors, the "smile curve" concept illustrates that the highest value-added activities—chip architecture and design, and the production of extreme ultraviolet (EUV) lithography equipment—are concentrated in a small number of firms in the United States, the Netherlands, and, for design software, a handful of specialized providers, while lower value-added activities such as assembly, testing, and packaging are more geographically dispersed and accessible to developing economies such as India, Vietnam, and Malaysia. This distribution of value-added activity has direct implications for which states can convert participation in the semiconductor supply chain into structural power, and which remain confined to lower-value, more substitutable segments of the network.

3.2 Weaponized Interdependence

Farrell and Newman's (2019) concept of weaponized interdependence provides an analytical lens for understanding how states occupying "hub" positions within global networks can exploit that position to coerce rivals. They distinguish between "panopticon effects," in which

hub states gain informational advantages, and "chokepoint effects," in which hub states can cut off network access to targeted actors. The United States' escalating export control regime on semiconductor manufacturing equipment and design software exemplifies chokepoint weaponization: because American firms and their close allies control critical nodes such as electronic design automation (EDA) software and extreme ultraviolet lithography, Washington has been able to restrict Chinese access to advanced chip fabrication capabilities even though the physical manufacturing occurs primarily in Taiwan and South Korea rather than on American soil.

3.3 Techno-Nationalism and Strategic Autonomy

The third strand, techno-nationalism, describes a policy orientation in which states treat technological capability as inseparable from national security and pursue deliberate strategies to reduce dependence on rival powers, even at the cost of economic efficiency. This orientation manifests in industrial policies such as the United States' CHIPS and Science Act, the European Chips Act, China's state-guided semiconductor investment funds, and India's Semicon India Programme. Techno-nationalism does not imply full autarky; rather, it typically produces a bifurcated or "friend-shored" pattern in which supply chains are reorganized around trusted alliance networks rather than purely cost-minimizing logics.

3.4 Integrated Framework

Combining these three strands, this paper conceptualizes the political economy of semiconductor supply chains as a contest over three interrelated dimensions: (1) positional power within the global production network, determined by control over high-value, hard-to-substitute nodes; (2) the capacity to weaponize interdependence by leveraging chokepoints against rivals; and (3) the political will and fiscal capacity to pursue techno-nationalist industrial policies aimed at reshaping the geographic distribution of production. This framework guides the empirical analysis that follows, particularly the assessment of India's strategy, which this paper argues represents an attempt to convert a peripheral position within the global production network into a more consequential one through targeted industrial policy and alignment with the "friend-shoring" strategies of established powers.

4. Methodology

This paper employs a qualitative, document-based analytical methodology appropriate for political economy research on rapidly evolving policy domains. The analysis draws on three categories of sources. First, primary policy documents, including government press releases, budget statements, and official mission documents from the Government of India's Ministry of Electronics and Information Technology, the India Semiconductor Mission, the United States Department of Commerce, and the European Commission, are used to establish the formal architecture of relevant industrial policies and export control regimes. Second, secondary analytical sources, including peer-reviewed academic literature, reports from established research institutions such as the Semiconductor Industry Association (SIA), the Centre for Strategic and International Studies (CSIS), the Observer Research Foundation (ORF), and ICRIER, are used to interpret and contextualize these developments. Third, industry and financial reporting on corporate investment decisions, such as those by Tata Electronics, Micron Technology, and TSMC, are used to substantiate empirical claims regarding the geographic distribution of manufacturing capacity.

The analysis is structured as a comparative case study design, examining the United States, China, Taiwan, and India as primary cases, with the European Union, Japan, and South Korea considered as secondary comparative cases. This design allows the paper to identify both

common patterns across techno-nationalist industrial strategies and country-specific variations shaped by differing resource endowments, technological starting points, and geopolitical alignments. Given the fast-moving nature of the subject matter, the paper prioritizes developments through 2026, while acknowledging that policy details are subject to continual revision. As with any analysis of an actively evolving policy domain, the specific figures and program details cited herein should be understood as reflecting the best available information at the time of writing and are subject to subsequent verification and updating.

5. The Global Semiconductor Value Chain: Structure and Chokepoints

5.1 Segmentation of the Value Chain

The semiconductor value chain can be analytically divided into four broad segments: design, fabrication (front-end manufacturing), assembly-test-and-packaging (back-end manufacturing, often termed OSAT), and the equipment and materials that enable each of these stages. Chip design is dominated by a combination of integrated device manufacturers, which both design and fabricate chips, and "fabless" firms that design chips but outsource fabrication to specialized foundries. American firms such as Qualcomm, Nvidia, Broadcom, and AMD dominate fabless design in advanced logic and graphics processing, while the underlying electronic design automation software required to design modern chips is itself concentrated among a small number of firms, predominantly based in the United States.

Fabrication, the capital-intensive process of physically manufacturing chips on silicon wafers, is where geographic concentration is most extreme. The most advanced logic nodes, at process geometries below ten nanometers, are manufactured almost exclusively by TSMC in Taiwan and, to a lesser extent, Samsung in South Korea. This concentration reflects the extraordinary capital costs of building leading-edge fabrication facilities, which can exceed twenty billion dollars per plant, combined with decades of accumulated process engineering expertise that is exceptionally difficult to replicate.

The equipment and materials segment, while less visible to the public, is arguably the most concentrated and therefore the most strategically significant node in the entire value chain. ASML, headquartered in the Netherlands, is the sole global supplier of extreme ultraviolet (EUV) lithography machines, which are indispensable for manufacturing the most advanced logic chips. This singular concentration means that any state seeking to restrict a rival's access to advanced chip fabrication can do so, in significant part, simply by controlling ASML's export licensing, a dynamic that has been central to the United States' coordinated export control strategy with the Netherlands and Japan.

5.2 Assembly, Testing, and Packaging

The final segment of the value chain, assembly, testing, and packaging, has traditionally been regarded as the least technologically sophisticated and most geographically mobile stage of semiconductor production. Historically concentrated in Southeast Asia, particularly Malaysia, the Philippines, and Taiwan, this segment has become an important entry point for new entrants to the semiconductor industry, including India, because it requires substantially lower capital investment and shorter development timelines than front-end fabrication. However, the emergence of advanced packaging technologies, which are increasingly important for high-performance computing and artificial intelligence applications, has begun to elevate the strategic significance of this segment, blurring the traditional distinction between "low-value" back-end operations and "high-value" front-end fabrication.

5.3 Chokepoints and Strategic Vulnerability

The concentration of critical capabilities in a small number of geographic locations and firms creates what political economists term chokepoints: nodes whose disruption, whether through natural disaster, geopolitical conflict, or deliberate export restriction, can produce cascading effects throughout the global economy. The COVID-19 pandemic-era semiconductor shortage of 2020 and 2021, which disrupted automobile and electronics production worldwide, provided a vivid demonstration of this vulnerability, and served as a catalyst for the wave of industrial policy responses examined in subsequent sections. The concentration of advanced fabrication in Taiwan, combined with the island's contested political status and its proximity to mainland China, represents the most consequential single point of vulnerability in the contemporary global economy, a theme explored further in Section 7.

6. United States-China Technological Rivalry and Export Controls

6.1 The Escalation of Export Controls

Since 2018, the United States has progressively restricted Chinese access to advanced semiconductor technology, motivated by concerns that Chinese acquisition of cutting-edge chips and chipmaking equipment could accelerate military modernization and artificial intelligence capabilities with dual-use military applications. Restrictions initially targeted specific firms, most notably the placement of Huawei Technologies on the Commerce Department's Entity List, which cut off the company's access to American semiconductor design software and manufacturing inputs. This firm-specific approach subsequently broadened into comprehensive, technology-based export controls covering advanced logic chips, high-bandwidth memory, and the equipment required to manufacture them, formalized in a series of rules issued by the Bureau of Industry and Security beginning in October 2022 and expanded in subsequent years.

A defining feature of this export control regime is its extraterritorial reach through the Foreign Direct Product Rule, which extends US jurisdiction to non-American firms that use American technology or software in their manufacturing processes. Because virtually all semiconductor manufacturing equipment incorporates some American-origin technology, this mechanism has enabled Washington to constrain the exports of allied firms, including the Netherlands' ASML and Japan's Tokyo Electron, notwithstanding these firms' formal independence from US jurisdiction. This dynamic exemplifies the weaponized interdependence framework discussed in Section 3, wherein the United States has converted its structural position within the global technology ecosystem into a coercive instrument against China, achieved substantially through allied coordination rather than unilateral action alone.

6.2 China's Response: State-Directed Self-Sufficiency

China's response to escalating export controls has centered on an ambitious, state-directed drive toward semiconductor self-sufficiency, most visibly embodied in the National Integrated Circuit Industry Investment Fund, colloquially known as the "Big Fund," which has channeled tens of billions of dollars into domestic semiconductor firms since its establishment in 2014, with successive funding rounds substantially expanding available capital. Beijing has also pursued a "whole nation" mobilization approach, integrating semiconductor development into broader strategic planning documents, including the "Made in China 2025" initiative and subsequent five-year plans, which explicitly identify semiconductor self-sufficiency as a national priority.

Despite this substantial investment, China's semiconductor industry continues to face significant constraints, particularly in advanced lithography, where domestic firms such as

Shanghai Micro Electronics Equipment (SMEE) remain generations behind ASML's EUV capabilities, and in electronic design automation software, where Chinese firms remain heavily dependent on tools produced by American companies such as Synopsys and Cadence, notwithstanding growing domestic alternatives. Chinese firms such as Semiconductor Manufacturing International Corporation (SMIC) have nonetheless demonstrated an ability to produce chips at more advanced process nodes than many analysts previously expected, reportedly using older deep ultraviolet lithography equipment through innovative multi-patterning techniques, illustrating both the resilience of China's engineering base and the practical limits of import substitution absent access to the most advanced equipment.

6.3 Structural Implications

The trajectory of United States-China semiconductor competition illustrates a broader pattern in which economic interdependence, rather than functioning as a stabilizing force in bilateral relations as classical liberal international relations theory would predict, has instead become a primary battleground of strategic competition. This dynamic has generated what several analysts describe as a process of "technological decoupling" or "de-risking," in which firms and governments increasingly prioritize supply chain resilience and geopolitical alignment over pure cost efficiency, a shift with direct implications for third countries such as India that are positioning themselves as alternative manufacturing locations.

7. Taiwan and the Silicon Shield

7.1 TSMC's Structural Centrality

No analysis of semiconductor political economy can proceed without sustained attention to Taiwan, and specifically to TSMC, which manufactures a substantial majority of the world's most advanced logic chips and serves as the principal foundry partner for leading fabless design firms including Apple, Nvidia, and AMD. TSMC's dominance did not emerge from state planning alone, though Taiwan's government played a significant catalytic role in the company's founding in 1987 through the state-backed Industrial Technology Research Institute; rather, it reflects decades of sustained investment in process engineering excellence, customer trust, and manufacturing scale that has proven exceptionally difficult for rivals, including Samsung and Intel, to replicate at the leading edge.

7.2 The Silicon Shield Thesis

Taiwan's concentration of advanced semiconductor manufacturing capability has given rise to what analysts term the "silicon shield" thesis: the argument that Taiwan's indispensability to the global technology ecosystem, and particularly to China's own electronics industry and to the United States' defense and technology sectors, creates a powerful deterrent against military conflict, since any disruption to TSMC's operations would impose catastrophic costs on all parties, including China itself, which remains a major customer of Taiwanese-manufactured chips despite the broader bilateral tension. Proponents of this thesis argue that Taiwan's semiconductor dominance has effectively internationalized the stakes of any potential conflict, embedding the island's security within the interests of the United States, Japan, and other technology-dependent economies.

Critics of the silicon shield thesis, however, caution that this logic may be double-edged: the same concentration that deters conflict by raising its costs could, in a crisis scenario, also incentivize a rapid military action intended to seize or neutralize Taiwan's semiconductor capacity before adversaries could respond, or alternatively could motivate the United States and its allies to accelerate diversification efforts precisely because reliance on a single contested territory is deemed unacceptably risky over the long term. This latter dynamic has

visibly shaped policy in Washington, Tokyo, and Brussels, each of which has pursued domestic and allied semiconductor manufacturing capacity expansion explicitly motivated by concerns over Taiwan Strait instability, including TSMC's own diversification investments in Arizona and Kumamoto, Japan.

7.3 Implications for Global Supply Chain Resilience

Taiwan's position thus embodies the central paradox of contemporary semiconductor political economy: the same concentration of capability that generates efficiency and technological leadership also generates acute systemic risk, incentivizing governments worldwide, including India, to pursue costly diversification strategies notwithstanding the near-term inefficiency of duplicating capabilities that already exist at scale in Taiwan. This dynamic forms the essential backdrop against which India's semiconductor strategy, examined in the following section, must be understood.

8. India's Emergence in Semiconductor Geopolitics

8.1 Historical Context and Motivations

India's engagement with semiconductor manufacturing has a longer and more troubled history than is commonly recognized. Early attempts at indigenous semiconductor fabrication, notably the Semiconductor Complex Limited established in Chandigarh (subsequently renamed the Semi-Conductor Laboratory) in 1976, achieved limited commercial success and were further set back by a major fire in 1989 that destroyed much of the facility's fabrication capacity. For subsequent decades, India's electronics industry remained heavily import-dependent, with domestic value addition concentrated in assembly rather than component manufacturing, contributing to what policymakers term India's "electronics trade deficit," a persistent gap between imports and exports of electronic goods that successive governments identified as a strategic and macroeconomic concern.

Several converging factors catalyzed India's renewed and substantially more ambitious semiconductor push beginning around 2021. First, the COVID-19 pandemic-induced global chip shortage exposed the risks of India's dependence on imported semiconductors for its automotive, telecommunications, and electronics industries. Second, escalating United States-China tensions created a strategic opening, as Western governments and firms actively sought to diversify supply chains away from China, a strategy often termed "China plus one" or "friend-shoring," and India, alongside Vietnam and Mexico, emerged as a prominent beneficiary of this reorientation. Third, India's own strategic planners, drawing on the precedent of successful electronics assembly localization achieved under the mobile phone manufacturing PLI scheme, sought to move up the value chain from assembly toward more sophisticated component manufacturing, including semiconductor fabrication itself.

8.2 Policy Architecture: The India Semiconductor Mission and PLI Schemes

The centerpiece of India's semiconductor strategy is the India Semiconductor Mission (ISM), established in December 2021 as a specialized business division under the Ministry of Electronics and Information Technology, with an original outlay of approximately ₹76,000 crore (roughly \$10 billion) dedicated to attracting investment across the semiconductor and display manufacturing ecosystem. The ISM's design reflects lessons drawn from the mixed record of earlier industrial policy efforts, adopting a fiscal incentive structure that provides capital subsidies of up to fifty percent of project cost for eligible semiconductor fabrication, display fabrication, and assembly-test-and-packaging facilities, with incentives disbursed on a milestone basis linked to demonstrated project progress rather than upfront grants, a design intended to mitigate the risk of subsidized projects failing to materialize.

Building on the initial phase of the mission, the Union Cabinet approved a substantially expanded second phase, Semicon India Programme 2.0, in mid-2026, with a reported outlay in the range of ₹1,27,500 crore. According to the government's own framing, ISM 2.0 represents a deliberate shift in strategic emphasis: whereas the first phase focused primarily on attracting fabrication and packaging facilities, the second phase is oriented toward deepening the supporting ecosystem, including semiconductor equipment and materials manufacturing, indigenous chip design intellectual property, and the specialty chemical and gas supply chains on which fabrication depends. This evolution reflects an emerging recognition among Indian policymakers that attracting individual manufacturing facilities, while a necessary first step, is insufficient to build genuine semiconductor sovereignty absent a deeper domestic ecosystem of suppliers, equipment providers, and skilled engineering talent.

8.3 Major Investment Projects

By 2026, India's semiconductor buildout had produced several concrete manufacturing projects, marking a transition from policy announcement to physical implementation. Micron Technology's Assembly, Test, and Packaging (ATMP) facility in Sanand, Gujarat, representing an investment of approximately ₹22,516 crore and supported by roughly \$825 million in government incentives, was inaugurated by Prime Minister Narendra Modi on 28 February 2026, becoming the first operational facility of the current mission cycle and processing DRAM and NAND memory products for mobile devices, data centers, and automotive applications. CG Power, in partnership with Japan's Renesas Electronics and Thailand's Stars Microelectronics, established an OSAT facility also located in Sanand, which similarly commenced commercial production in early 2026. Kaynes Semicon, a facility that shipped India's first commercially packaged multi-chip modules to an American client in October 2025, was likewise inaugurated as an operational facility during this period.

The most consequential and technologically significant project remains the Tata Electronics facility at Dholera, Gujarat, developed in partnership with Taiwan's Powerchip Semiconductor Manufacturing Corporation (PSMC). Representing an estimated investment of approximately ₹91,000 crore, the Dholera facility is designed as India's first front-end wafer fabrication plant, targeting a production capacity of 50,000 wafers per month at process nodes of 28 nanometers and above. While these process nodes are several generations behind the sub-ten-nanometer capabilities of TSMC's most advanced facilities, they remain highly relevant for automotive electronics, power management chips, industrial microcontrollers, display drivers, and defense applications, representing a pragmatic entry point for India into front-end fabrication rather than an attempt to compete directly at the technological frontier. As of mid-2026, the Dholera facility was targeting first silicon production by late 2026, with full commercial-scale fabrication capability projected for 2028. Complementing this front-end investment, Tata Electronics has also developed a large-scale OSAT facility in Jagiroad, Assam, with a stated packaging capacity of up to 48 million chips per day, reflecting a deliberate strategy of building both front-end and back-end capabilities within an integrated domestic ecosystem, and extending semiconductor investment beyond the traditionally dominant western state cluster into India's northeastern region.

8.4 Structural Constraints and Implementation Challenges

Notwithstanding these advances, India's semiconductor strategy confronts substantial structural constraints that merit sober analytical treatment rather than uncritical celebration. Budgetary analysis conducted by parliamentary research bodies has noted meaningful underutilization of allocated funds relative to budgeted expenditure, a pattern attributable in part to the milestone-linked disbursement structure of the incentive scheme, which necessarily produces a lag between fiscal allocation and actual expenditure given the multi-year

construction timelines characteristic of semiconductor fabrication facilities. As of 2026, only three of twelve approved commercial semiconductor units had commenced commercial production, with India's first front-end fabrication facility not expected to reach full-scale operation until 2028, illustrating the considerable gap between policy ambition and realized manufacturing capability that characterizes any nascent semiconductor industry.

More fundamentally, India's current cluster of investments is concentrated overwhelmingly in mature process nodes and back-end assembly, testing, and packaging operations rather than the leading-edge fabrication capabilities that dominate strategic discourse around artificial intelligence and advanced computing. India also remains heavily dependent on imported specialty chemicals, ultra-pure gases, photoresists, photomasks, and precision manufacturing equipment, an equipment and materials ecosystem that domestic industry has not yet developed, and which the government's own ISM 2.0 framework explicitly identifies as the critical missing layer of the domestic value chain. Talent availability represents a further constraint: while the government reports having trained approximately 70,000 students across 320 universities in electronic design automation tools, the specialized workforce required for cleanroom operation, fabrication process engineering, and advanced packaging remains in short supply relative to the scale of ambition articulated in government planning documents, necessitating continued reliance on foreign technical partners such as PSMC in the near to medium term.

8.5 India's Strategic Positioning Within Great Power Competition

India's semiconductor strategy cannot be understood in isolation from the broader dynamics of United States-China competition examined in Section 6. India has benefited substantially from the "China plus one" diversification strategy pursued by Western governments and multinational corporations seeking to reduce geopolitical and supply chain risk associated with overreliance on Chinese manufacturing. This positioning aligns with India's participation in minilateral technology cooperation frameworks such as the India-United States initiative on Critical and Emerging Technology (iCET), through which the two governments have sought to deepen collaboration on semiconductor supply chain resilience, among other advanced technology domains.

At the same time, India's semiconductor ambitions reflect a distinctively autonomous strategic logic rather than simple alignment with any single great power bloc, consistent with India's longstanding foreign policy tradition of strategic autonomy. Indian policymakers have consistently framed the semiconductor mission in terms of reducing the country's own dependence on any single external supplier, a formulation that applies equally to China and, implicitly, to overreliance on any single Western partner. This positioning allows India to simultaneously benefit from Western diversification strategies while pursuing an independent long-term objective of building indigenous technological capability, a posture consistent with India's broader approach to great power competition across multiple domains, including its participation in both the Quadrilateral Security Dialogue with the United States, Japan, and Australia, and its continued engagement with multilateral institutions in which China plays a significant role.

9. Comparative Analysis: Semiconductor Strategies Across Major and Emerging Powers

9.1 The United States: From Market Leadership to Reindustrialization

The United States retains overwhelming dominance in chip design and electronic design automation software but has experienced significant erosion of its domestic manufacturing base over recent decades, with the share of global semiconductor manufacturing capacity located

within the United States having declined substantially since the 1990s. The CHIPS and Science Act of 2022, providing approximately \$52 billion in manufacturing incentives and research funding, represents Washington's principal legislative response, aimed at reshoring advanced fabrication capacity, exemplified by TSMC's, Samsung's, and Intel's respective investments in new fabrication facilities in Arizona, Texas, and Ohio. This strategy combines defensive elements, restricting Chinese access to advanced technology, with offensive elements, subsidizing domestic and allied manufacturing capacity, reflecting a comprehensive technological nationalist industrial policy that marks a significant departure from the laissez-faire orientation that characterized much of American technology policy in preceding decades.

9.2 China: Import Substitution Under Constraint

As detailed in Section 6, China's strategy centers on state-directed investment aimed at achieving self-sufficiency across the semiconductor value chain, an objective rendered more urgent by escalating export controls but constrained by the technological gap in advanced lithography and electronic design automation software that domestic firms have not yet closed. China's approach illustrates both the potential and the limits of state-directed industrial policy: substantial progress has been achieved in mature-node manufacturing and in specific niches such as compound semiconductors, but the most advanced process nodes remain largely inaccessible absent a breakthrough in indigenous lithography capability.

9.3 The European Union: Coordinated Subsidy Without Manufacturing Scale

The European Chips Act, adopted in 2023, mobilizes approximately €43 billion in public and private investment aimed at doubling the European Union's share of global semiconductor manufacturing capacity to twenty percent by 2030. The European strategy is distinguished by its emphasis on preserving and expanding the region's existing strengths in semiconductor equipment manufacturing, exemplified by ASML, and in automotive and industrial chips, rather than attempting to establish leading-edge logic fabrication capacity from a limited existing base, reflecting a more targeted and resource-constrained approach relative to the more comprehensive ambitions articulated by the United States and China.

9.4 Japan and South Korea: Established Players Navigating Realignment

Japan, historically a dominant force in semiconductor manufacturing during the 1980s before losing substantial market share to South Korean and Taiwanese competitors, has pursued an ambitious reindustrialization strategy centered on the state-backed Rapidus consortium, which aims to establish domestic leading-edge logic fabrication capability by the end of the decade, alongside continued strength in semiconductor materials and equipment manufacturing. South Korea, home to Samsung Electronics and SK Hynix, retains substantial manufacturing scale, particularly in memory chips, but faces mounting pressure from both Chinese competition in mature-node memory production and American export controls affecting its operations in China, illustrating the difficult positioning confronted by established semiconductor powers with substantial commercial exposure to the Chinese market.

9.5 India's Distinctive Positioning

Situated against this comparative landscape, India's strategy is distinguished by several features. First, India entered the contemporary phase of semiconductor competition later than its comparators, with concrete manufacturing investment materializing only from 2023 onward, reflecting India's historically limited semiconductor manufacturing base. Second, India's strategy has deliberately prioritized back-end assembly, testing, and packaging alongside mature-node front-end fabrication, a pragmatic sequencing that leverages India's

existing strengths in electronics assembly and lower labor costs while building toward more advanced capabilities over a longer time horizon, rather than attempting to compete immediately at the technological frontier occupied by Taiwan and, prospectively, the United States, Japan, and South Korea. Third, India's strategy is distinctively integrated with its broader digital economy ambitions, reflected in the emphasis placed on developing indigenous chip design capability to serve India's large and rapidly growing domestic electronics and telecommunications market, an emphasis less pronounced in the strategies of smaller, more export-oriented economies. This comparative positioning suggests that India occupies a distinctive niche within the broader global reconfiguration of semiconductor supply chains: neither a leading-edge technology power in the near term, nor a purely passive beneficiary of diversification strategies pursued by others, but rather an emerging manufacturing hub attempting to convert temporary geopolitical opportunity into durable, indigenous technological capability.

10. Discussion: Broader Political Economy Implications

10.1 The Fragmentation of Global Technology Markets

The cumulative effect of the developments examined in this paper is the gradual fragmentation of what was, until recently, a highly globalized and efficiency-optimized semiconductor market into increasingly distinct, geopolitically aligned technology blocs. This fragmentation carries substantial economic costs, as duplicative manufacturing investment across multiple jurisdictions necessarily sacrifices the economies of scale and specialization that historically drove down semiconductor costs and accelerated innovation. Estimates from industry associations and economic research institutions have suggested that a fully "decoupled" semiconductor supply chain, in which the United States and China pursue fully independent manufacturing ecosystems, could impose meaningfully higher costs on chip production and end-user electronics prices globally, alongside slower rates of technological advancement due to reduced economies of scale and diminished cross-border knowledge diffusion.

10.2 Implications for Developing and Emerging Economies

For developing and emerging economies such as India, the fragmentation of global semiconductor supply chains presents a double-edged strategic opportunity. On one hand, the diversification strategies pursued by Western governments and firms create genuine openings for new entrants to capture manufacturing investment that would, under a purely cost-optimizing logic, have continued to concentrate in existing East Asian hubs. On the other hand, this opportunity is inherently contingent on the continuation of great power tensions and Western diversification preferences, raising questions about the durability of investment commitments should geopolitical circumstances shift, and about the risk that emerging economies could become locked into geopolitically motivated but commercially suboptimal positions within global production networks, dependent on continued political rather than purely economic logic for their competitive position.

10.3 The Limits of Techno-Nationalist Industrial Policy

The comparative analysis in Section 9 also illustrates the significant limits of techno-nationalist industrial policy, even when backed by substantial fiscal resources. China's experience demonstrates that state investment alone cannot readily substitute for decades of accumulated process engineering expertise and access to specialized equipment controlled by a small number of firms concentrated in allied jurisdictions. India's experience similarly illustrates the multi-year, and in the case of leading-edge fabrication, potentially multi-decade timelines required to build credible domestic semiconductor manufacturing capability, even under conditions of substantial fiscal support and favorable geopolitical tailwinds. These findings

collectively suggest that while techno-nationalist industrial policy can meaningfully reshape the geographic distribution of manufacturing investment, particularly at mature process nodes and in back-end operations, the reproduction of leading-edge capabilities currently concentrated in Taiwan is likely to remain an exceptionally difficult and slow undertaking for any single state, however well-resourced.

10.4 Semiconductor Competition and the Broader International Order

Finally, the political economy of semiconductor supply chains offers a revealing window into the broader trajectory of the contemporary international order. The subordination of commercial efficiency to strategic autonomy considerations, evident across the cases examined in this paper, reflects a wider retreat from the assumptions of economic interdependence that characterized the post-Cold War liberal international order, replaced by an emerging paradigm in which economic relationships are increasingly evaluated through the lens of strategic risk and alliance alignment. Whether this fragmentation ultimately produces a more stable, if less efficient, multipolar technology order, or instead generates new sources of instability and conflict risk, particularly given Taiwan's continued centrality, remains one of the defining uncertainties of contemporary international political economy.

11. Policy Recommendations

Drawing on the preceding analysis, several policy implications emerge, particularly relevant to India's continued semiconductor development.

First, sustained and predictable fiscal commitment is essential given the multi-year investment horizons characteristic of semiconductor manufacturing; policy discontinuity or funding uncertainty risks undermining investor confidence built through the initial phase of the India Semiconductor Mission. Second, the transition toward ISM 2.0's emphasis on equipment, materials, and design intellectual property represents an appropriate strategic sequencing, and should be pursued with particular attention to developing domestic capability in specialty chemicals and gases, an area where India remains almost entirely import-dependent. Third, talent development initiatives should be substantially scaled beyond current levels, with particular emphasis on practical, industry-embedded training in fabrication process engineering rather than purely theoretical instruction, given the acute shortage of experienced semiconductor manufacturing personnel documented in Section 8.4. Fourth, India should continue to pursue diversified international partnerships, engaging simultaneously with Taiwanese, American, Japanese, and European firms and governments, in order to avoid excessive dependence on any single foreign technology partner, consistent with the strategic autonomy logic that has historically characterized Indian foreign policy. Finally, policymakers should maintain realistic expectations regarding timelines for achieving leading-edge fabrication capability, recognizing that India's near-to-medium-term comparative advantage lies substantially in mature-node fabrication and back-end assembly, testing, and packaging operations, with leading-edge capability representing, at best, a longer-term aspiration contingent on successful development of the broader supporting ecosystem.

12. Limitations and Directions for Future Research

This paper is subject to several limitations that merit acknowledgment. First, given the rapidly evolving nature of semiconductor policy and geopolitics, specific figures and program details are subject to continual revision, and readers should consult current primary sources for the most up-to-date information. Second, the qualitative, document-based methodology employed here, while appropriate for a topic characterized by rapid change and limited availability of granular firm-level data, does not permit the kind of quantitative causal inference that would

be required to precisely estimate the economic effects of specific policy interventions. Future research employing quantitative trade and investment data, once sufficient time series become available following the recent wave of policy interventions, could usefully test some of the propositions advanced in this paper, particularly regarding the durability of investment flows attracted by diversification-driven industrial policy. Additionally, future research would benefit from more granular firm-level case studies of specific Indian semiconductor investments, examining in greater depth the technology transfer arrangements, workforce development outcomes, and supply chain localization achieved by projects such as the Tata-PSMC partnership at Dholera, as these projects mature and generate more extensive operational track records.

13. Conclusion

This paper has examined the political economy of semiconductor supply chains as a defining arena of contemporary great power competition, integrating global production network theory, weaponized interdependence, and techno-nationalist industrial policy theory into a unified analytical framework. The analysis demonstrates that the semiconductor industry's extreme geographic and firm-level concentration, a product of decades of efficiency-driven corporate strategy, has become a source of profound strategic vulnerability that governments worldwide are now attempting to address through unprecedented levels of industrial policy intervention. The United States' escalating export control regime, China's state-directed pursuit of self-sufficiency, and Taiwan's precarious but strategically consequential centrality collectively illustrate a broader shift from commercially optimized global production networks toward increasingly fragmented, geopolitically aligned technology blocs.

Within this reconfiguring landscape, India's emergence as a significant, if still nascent, semiconductor manufacturing location represents a distinctive and analytically underexplored case. India's strategy, embodied in the India Semiconductor Mission and its associated investment projects at Sanand, Dholera, and Jagiroad, illustrates both the genuine opportunities created by great power competition for strategically positioned emerging economies and the substantial structural constraints, spanning equipment dependence, talent shortages, and the multi-year timelines inherent to semiconductor manufacturing, that continue to limit the pace at which such opportunities can be converted into durable technological capability. As the global semiconductor order continues to fragment along geopolitical lines, India's experience offers valuable lessons for other emerging economies seeking to navigate the opportunities and risks created by the ongoing reconfiguration of the world's most strategically consequential industry.

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